REMARKS

This RCE responds to the Advisory Office Action mailed on May 5, 2008. No new matter was added by these amendments.

§103 Rejection of the Claims

Claims 1, 2, 4, 5, 7, 10-12, 14, 15 and 17-19 were rejected under 35 USC § 103(a) as being unpatentable over Jacobson et al. (U.S. 6,517,995) in view of Suda et al. (U.S. 4,731,855) and Kamieniecki et al. (U.S. 5,661,408).

In the ***Response to Arguments***, the Final Office Action asserts:

> The Examiner respectfully disagrees with this argument. First of all, Suda and Kamieniecki were cited by the Examiner **only** to show that **in-line or *in-situ* testing was known in the art** *of manufacturing semiconductor devices for e.g. fast testing of patterns on semiconductor wafers, etc. to reduce the financial losses resulting from errors.* The Examiner

The Applicant believes that the citation to reference for a narrow purpose which fails to recognize what the reference teaches, is improper use of that reference. This action amounts to impermissible hindsight. Where the Office asserts it was known to fast test patterns on *semiconductor wafers*, the Applicant respectfully replies, the Applicant is not claiming a process having to do with semiconductor wafers.

If this statement from the Office is parsed such that the "etc" is removed, the statement cannot be supported to render obvious processing and testing of printed wiring boards. "[I]n situ testing was known in the art of manufacturing semiconductive devices for e.g. fast testing of patterns on semiconductor wafers" is not the scope of what is claimed. Where the Office Action inserts "*etc.*" in the phrase "known to fast test patterns on *semiconductor wafers, etc.*" The Applicant believes this "*etc.*" is a catch-all to assert something that is not plainly taught or suggested in the combined references and in particular, what is claimed.

The Final Office Action asserts:

> *semiconductor wafers, etc. to reduce the financial losses resulting from errors.* The Examiner never addressed the testing techniques because they were not recited in claims. Therefore, in

The Applicant believes, however, the pending claims do recite testing techniques, *e.g.*, "in situ *testing a board layout on the PWB [an imprinted polymer] while attached as part of an array of*

[imprinted polymer]PWBs." (Claim 1). This language of "imprinted polymer" to define the printed wiring board is in the plain text of claim 1. Consequently, where the Applicant claims such a combination, and the cited references, Suda and Kamieniecki have nothing to do with what is claimed, the disconnect lies between Jacobson and the Suda and Kamieniecki references, where Jacobson's technology if applied to either of Suda or Kamieniecki, would destroy such inventions. Further, the "substrate" of Jacobson is not the "substrate" of either of Suda or Kamieniecki.

The Final Office Action asserts:

> never addressed the testing techniques because they were not recited in claims. Therefore, in contrast to Applicants assertion, neither Jacobson's technology was applied to either Suda or Kamieniecki nor testing techniques of Suda or Kamieniecki were applied to Jacobson.

The Applicant believes this amounts to an assertion the references are submitted in the vacuum of ignoring how and why Suda or Kamieniecki teach their technologies, which run afoul of Jacobson's technologies and teachings. And further, this assertion ignores the disparate substrates, but the Applicant has claimed an imprinted polymer substrate in the process claims.

Consequently, merely that either of Suda or Kamieniecki may teach testing of their semiconductor wafer substrates, fails to show a teaching or suggestion to combine their technologies with Jacobson to suggest a teaching of "in situ *testing a board layout on the PWB [an imprinted polymer] while attached as part of an array of [imprinted polymer]PWBs.*" (Claim 1). Further, Jacobson would not look to either of Suda or Kamieniecki to solve any technical challenges or fields of endeavor. Withdrawal of the rejections is respectfully requested.

Claims 1, 2, 4-12, 14-20 and 31-36 were also rejected under 35 USC § 103(a) as being unpatentable over Carter (U.S. 6,730,617) in view of Suda et al. and Kamieniecki et al.

The Office admits that "Carter fails to teach in situ testing the substrate while attached as part of an array of substrates." Applicant agrees. To that end, the Office has proffered Suda and Kamieniecki. But these references have nothing to do with what is claimed. Similarly to the above rejection involving Jacobson, the disconnect lies between Carter and the Suda and

Kamieniecki references, where Carter's technology if applied to either of Suda or Kamieniecki, would destroy such inventions. Further, the "substrate" of Carter is not the "substrate" of either of Suda or Kamieniecki. Consequently, merely that of either of Suda or Kamieniecki may teach testing of their substrates, fails to show a teaching or suggestion to combine their technologies with Jacobson. Further, Carter would not look to either of Suda or Kamieniecki to solve any technical challenges or fields of endeavor. Withdrawal of the rejections is respectfully requested.

Claims 3, 6, 20 and 31-33 were also rejected under 35 USC § 103(a) as being unpatentable over Jacobson et al. in view of Suda et al. and Kamieniecki et al., and further in view of Bulthaup et al. (U.S. 6,936,181).

The above traversal involving the combination of Jacobson with either of both or Suda or Kamieniecki is incorporated herein by reference. The Office again refers to Paragraph 10 of a previous Office Action that admits "Jacobsen et al fail to teach in situ testing the substrate while attached as part of an array of substrates." Applicant agrees. But Bulthaup also fails to teach this limitation. Because all the claim limitations are not taught by the cited references, withdrawal of the rejections is respectfully requested. (M.P.E.P. § 2143 8th Ed, Rev.4).

Claim 3 was also rejected under 35 USC § 103(a) as being unpatentable over Jacobson et al. in view of Suda et al. and Kamieniecki et al./Carter, and further in view of Walter (US 4099913).

The above traversal involving the combination of Jacobson with either of both or Suda or Kamieniecki is incorporated herein by reference. Applicant believes Jacobsen et al fail to teach in situ testing a board layout on the array of PWBs while not singulated from the array of substrates. A previous Office Action also admits "Jacobson fails to teach in situ testing the substrate while attached as part of an array of substrates." Applicant agrees. But Walter also fails to teach this limitation. Because all the claim limitations are not taught by the cited references, withdrawal of the rejections is respectfully requested. (M.P.E.P. § 2143 8th Ed, Rev.4).

Claims 6, 8, 9, 16, 20, 31, 32 and 34-36 rejected under 35 USC § 103(a) as being unpatentable over Jacobson et al. in view of Suda et al. and Kamieniecki et al., and further in view of Carter.

The above traversals involving the combination of either of Jacobson or Carter with either of both or Suda or Kamieniecki are incorporated herein by reference. A previous Office also Action that admits "Carteret al fail to teach in situ testing the substrate while attached as part of an array of substrates." Applicant agrees.

This rejection represents an aggregation of references that fail to teach or suggest the limits of the claims. Jacobson in view of Suda or Kamieniecki fail to teach what is claimed since combination of the references results in one meaning of "substrate" (e.g. Jacobson's substrate) that is repugnant to either of Suda or Kamieniecki's substrate. Carter in view of Suda or Kamieniecki fail to teach what is claimed since combination of the references results in one meaning of "substrate" (e.g. Carter's substrate) that is repugnant to either of Suda or Kamieniecki's substrate.

Because all the claim limitations are not taught by the cited references, withdrawal of the rejections is respectfully requested. (M.P.E.P. § 2143 8th Ed, Rev.4).

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all

rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((503) 712-3485) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-0221.

Respectfully submitted,

SAIKUMAR JAYARAMAN

By his Representatives,

By /  /
John N. Greaves
Reg. No. 40,362